What is claimed is:

1. A semiconductor device comprising:

a first MOSFET including:

a first gate electrode formed on a first semiconductor layer in a first region of a semiconductor substrate;

a first channel region formed immediately below said first gate electrode in the first semiconductor layer;

a first diffusion layer constituting source/drain regions formed at both the sides of said first channel region in the first semiconductor layer;

a first epitaxial layer formed on said first diffusion layer; and

a first silicide layer formed on said first epitaxial layer; and

a second MOSFET including:

a second gate electrode formed on a second semiconductor layer in a second region of the semiconductor substrate;

a second channel region formed immediately below said second gate electrode in the second semiconductor layer;

a second diffusion layer constituting source/drain regions formed at both the sides of said second channel region in the second semiconductor layer; and

a second silicide layer formed on said second diffusion layer.

2. The semiconductor device according to claim 1, wherein:

said first MOSFET includes a third diffusion layer formed between said first channel region and said first diffusion layer in the first semiconductor layer and having a lower impurity concentration than said first diffusion layer; and

said second MOSFET includes a fourth diffusion layer formed between said second channel region and said second diffusion layer in the second semiconductor layer and having a lower impurity concentration than said second diffusion layer.

3. The semiconductor device according to claim 1, wherein the second semiconductor layer contains silicon, and said second diffusion layer of said second MOSFET contains carbon.

4. The semiconductor device according to claim 1, wherein said first region is an SOI region, and said second region is a bulk region.

5. The semiconductor device according to claim 1, wherein said first MOSFET is a p-channel MOSFET, and said second MOSFET is an n-channel MOSFET.

6. A semiconductor device comprising:

a first MOSFET including:

a first gate electrode formed on a first semiconductor layer in a first region of a semiconductor substrate;

a first channel region formed immediately below said first gate electrode in the first semiconductor layer;

a first diffusion layer constituting source/drain regions formed at both the sides of said first channel region in the first semiconductor layer;

a first epitaxial layer formed on said first diffusion layer; and

a first silicide layer formed on said first epitaxial layer; and

a second MOSFET including:

a second gate electrode formed on a second semiconductor layer in a second region of the

semiconductor substrate;

a second channel region formed immediately below said second gate electrode in the second semiconductor layer;

a second diffusion layer constituting source/drain regions formed at both the sides of said second channel region in the second semiconductor layer;

a second epitaxial layer, which is thinner than said first epitaxial layer, formed on said second diffusion layer; and

a second silicide layer formed on said second epitaxial layer.

7. The semiconductor device according to claim 6, wherein:

said first MOSFET includes a third diffusion layer formed between said first channel region and said first diffusion layer in the first semiconductor layer and having a lower impurity concentration than said first diffusion layer; and

said second MOSFET includes a fourth diffusion layer formed between said second channel region and said second diffusion layer in the second semiconductor layer and having a lower impurity concentration than said second diffusion layer.

8. The semiconductor device according to claim 6, wherein the second semiconductor layer contains silicon, and said second diffusion layer of said second MOSFET contains carbon.

9. The semiconductor device according to claim 6, wherein said first region is an SOI region, and said second region is a bulk region.

10. The semiconductor device according to claim 6, wherein said first MOSFET is a p-channel MOSFET, and said second MOSFET is an n-channel MOSFET.

11. A method of manufacturing a semiconductor device comprising:

forming a first gate electrode on a first semiconductor layer in a first region of a semiconductor substrate, and a second gate electrode on a second semiconductor layer in a second region of the semiconductor substrate;

forming a first diffusion layer in said first semiconductor layer using said first gate electrode as a mask, and a second diffusion layer in said second semiconductor layer using said second gate electrode as a mask; and

selectively forming an epitaxial layer only on said first diffusion layer.

12. The method of manufacturing a semiconductor device according to claim 11, wherein said first region is an SOI region, and said second region is a bulk region.

13. The method of manufacturing a semiconductor device according to claim 11, wherein said selective forming of the epitaxial layer includes:

forming an oxide layer on the surface of said second diffusion layer in said second region by emitting O_2 plasma with only said first region being masked; and

subsequently forming said epitaxial layer by epitaxial growth on said first diffusion layer.

14. The method of manufacturing a semiconductor device according to claim 11, further including:

implanting carbon into said first and second diffusion layers before forming said epitaxial layer,

wherein said selective forming of the epitaxial layer includes:

forming an oxide layer on the surface of said first diffusion layer in said first region by emitting O_2 plasma with only said second region being masked;

removing the mask, and then removing said oxide layer;

and

subsequently forming said epitaxial layer by epitaxial growth on said first diffusion layer.

15. The method of manufacturing a semiconductor device according to claim 14, wherein said implanting carbon is performed by forming first and second gate sidewalls at side portions of said first and second gate electrodes through the RIE method using carbon gas as an active gas.

16. The method of manufacturing a semiconductor device according to claim 11, further including forming silicide layer by performing silicidation of the surface of said epitaxial layer on said first diffusion layer and said second diffusion layer.

17. The method of manufacturing a semiconductor device according to claim 11, including further forming an epitaxial layer on said first diffusion layer and forming an epitaxial layer on said second diffusion layer by the epitaxial growth method.

18. The method of manufacturing a semiconductor device according to claim 17, further including performing silicidation of said epitaxial layers on said first diffusion layer and said second diffusion layer.